EVB-LAN8700

LAN8700(I) MII Customer Evaluation Board

+3.3V I/O VDDIO Operation

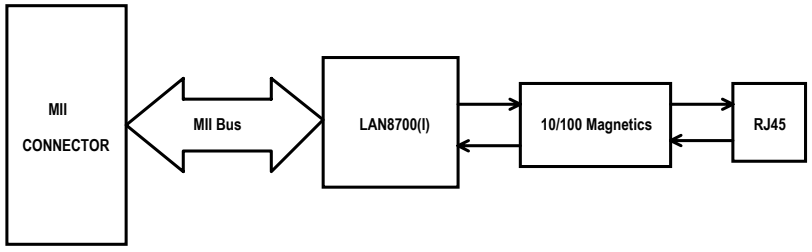
Schematic Revision E0P1

Design Details

Board: PCB-7054AZ-E0
Chip: LAN8700(I)
Board Form Factor:
Assembly:

Circuit Diagrams utilizing SMSC Products Are Included As A Means Of Illustrating Typical Semiconductor Applications: Consequently Complete Information Sufficient For Construction Purposes Is Not Necessarily Given. The Information Has Been Carefully Checked And Is Believed To Be Entirely Reliable. However, No Responsibility Is Assumed For Inaccuracies. Furthermore, Such Information Does Not Convey To The Purchaser Of The Semiconductor Devices Described Any License Under The Patent Rights Of SMSC Or Others. SMSC Reserves The Right To Make Changes At Any Time In Order To Improve Design And Supply The Best Product Possible.

EVB BLOCK DIAGRAM



ITEM	Page
Title Page	1
Stackup and Layout	2
LAN8700(I) & Magnetics	3
Power & Misc	4

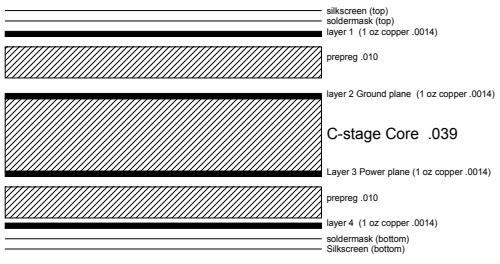
Revisions

Rev D1	12/6/05	Customer Public version created from D1
Rev D2	12/12/05	Corrected for the industrial temp capacitance
Rev D3	12/15/05	Corrected for REGOFF pin polarity change
Rev D4	1/16/06	INTR to header; increased test header to 24p intr to vddio; moved .01uf to vddio and added 10uf to vddio; added intersheet references.
Rev E0	2/24/06	Reference Design for A0 silicon with +3.3V I/O VDDIO
Rev E0P1	5/11/06	EVB revision E0 Public version 1: added strapping resistors to PHY address table on page 3

SMSC SUCCESS BY DESIGN
3930 East Ray Road
Suite 200
Phoenix, Arizona 85044
480-759-0200

Title: LAN8700(I) MII EVB
Size: C | Document Number: SCH-7054AZ | Rev: E0P1
Date: Wednesday, January 06, 2010 | Sheet 1 of 4

stackup

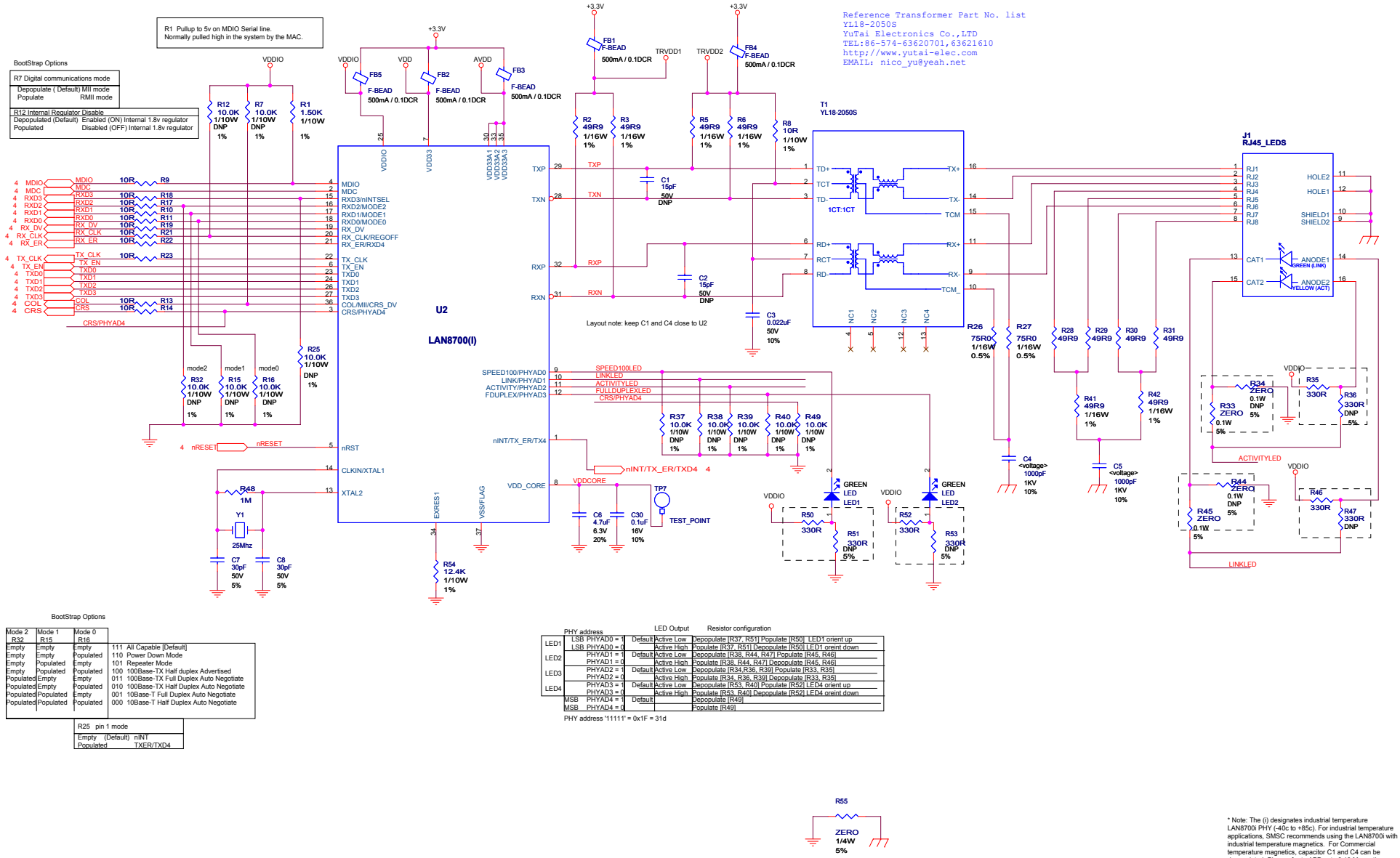


NOTES:

1. BOARD FABRICATION AND QUALITY ACCEPTANCE PER IPC-6012 CLASS 2. BOARD MUST MEET OR EXCEED QUALIFICATION TESTING AND QUALITY CONFORMACE TESTING INSPECTION SPECIFIED WITHIN.
2. MATERIAL: NEMA GRADE STANDARD FR4. LAMINATED SHEET, HTE 1 OZ COPPER CLAD, TYPE GF/GFG WOVEN GLASS BASE, FLAME RESISTANCE MEETING UL94V-0 OR BETTER. MATERIAL IN ACCORDANCE WITH IPC-4101.
3. BOARD FABRICATION SHALL APPLY DATE CODE, FABRICATOR'S CAGE CODE, I.D. AND UL MARKING TO SECONDARY SIDE WHERE INDICATED. MARKING PREFERABLY COPPER ETCHED. EPOXY INK ACCEPTABLE.
4. SOLDERMASK,USING TYPEB,PHOTO IMAGEABLE LPI FILM 0.0015 THICK. APPLY TO BOTH SIDES IN ACCORDANCE WITH IPC-SM-840 (TYPE B CLASS 3). USE APPROPIATE SOLDER MASK ARTWORK FOR EACH SIDE. PUNCTURING OF PUNCTURING OF TENTED HOLES IS PERMISSIBLE. SOLDERMASK MISREGISTRATION SHALL NOT EXCEED .004 INCH. SOLDERMASK OVERLAP PERMITTED ON CIRCULAR LANDS ONLY AND SHALL NOT EXCEED 0.001 INCH. NO OVERLAP PERMITTED ON RECTANGULAR LANDS.
5. FINISH: SOLDER MASK OVER BARE COPPER (SMOBC), HOT AIR LEVEL DEPOSIT
6. DRILL BOARDS USING DRILL DATA, DRILL PATTERN AND HOLE SCHEDULE. HOLE LOCATION MAY VARY WITHIN .004 IN. MAX ABOUT TRUE POSITION.
7. MINIMUM ANNULAR RINGS:
   .002 IN MINIMUM - EXTERNAL LAYERS.
   .001 IN MINIMUM - INTERNAL LAYERS.
8. ALL EXPOSED SURFACE LANDS AND LINES TO BE SOLDER COATED.
9. ALL HOLES ARE PLATED THROUGH UNLESS NOTED OTHERWISE. MINIMUM COPPER PLATING IN PLATED HOLES TO BE .001 IN. COPPER PLATING IN TENTED HOLES SHALL NOT PLUG HOLES WITHOUT PERMISSION FROM SMSC.
10. COMPONENT MARKINGS: SILKSCREEN BOTH SIDES USING NON-CONDUCTIVE WHITE EPOXY INK. LANDS AND EXPOSED PLATED AREAS TO BE FREE OF INK.
11. DIMENSIONS ARE AFTER ETCHING AND PLATING AND ARE BASIC UNLESS OTHERWISE INDICATED.
12. BARE BOARD ELECTRICAL TEST: BARE BOARDS SHALL BE ELECTRICALLY TESTED USING CAD GENERATED NET LIST DATA. THIS INFORMATION TO BE SUPPLIED IN IPC-D-356 FORMAT. ELECTRICAL TESTING SHALL FOLLOW THE GUIDELINES EXTABLISHED BY IPC-ET-652. GUIDELINES AND REQUIREMENTS FOR ELECTRICAL TESTING OF PRINTED WIRING BOARDS.

SMSC
SUCCESS BY DESIGN
3930 East Ray Road
Suite 200
Phoenix, Arizona 85044
480-759-0200

Title		
LAN8700(i) MII EVB		
Size: C	Document Number: SCH-7054AZ	Rev: E0P1
Date: Wednesday, January 06, 2010	Sheet 2 of 4	



BootStrap Options

Mode 2 R32	Mode 1 R15	Mode 0 R16	
Empty	Empty	Empty	111 All Capable [Default]
Empty	Empty	Populated	110 Power Down Mode
Empty	Populated	Empty	101 Repeater Mode
Empty	Populated	Populated	100 100Base-TX Half duplex Advertised
Populated	Empty	Empty	011 100Base-TX Full Duplex Auto Negotiate
Populated	Empty	Populated	010 100Base-TX Half Duplex Auto Negotiate
Populated	Populated	Empty	001 10Base-T Full Duplex Auto Negotiate
Populated	Populated	Populated	000 10Base-T Half Duplex Auto Negotiate

R25 pin 1 mode	
Empty (Default)	nINT
Populated	TXER/TXD4

	PHY address		LED Output	Resistor configuration
LED1	LSB PHYAD0 = 1	Default	Active Low	Depopulate [R37, R51] Populate [R50] LED1 orient up
	LSB PHYAD0 = 0		Active High	Populate [R37, R51] Depopulate [R50] LED1 oreint down
LED2	PHYAD1 = 1	Default	Active Low	Depopulate [R38, R44, R47] Populate [R45, R46]
	PHYAD1 = 0		Active High	Populate [R38, R44, R47] Depopulate [R45, R46]
LED3	PHYAD2 = 1	Default	Active Low	Depopulate [R34,R36, R39] Populate [R33, R35]
	PHYAD2 = 0		Active High	Populate [R34, R36, R39] Depopulate [R33, R35]
LED4	PHYAD3 = 1	Default	Active Low	Depopulate [R53, R40] Populate [R52] LED4 orient up
	PHYAD3 = 0		Active High	Populate [R53, R40] Depopulate [R52] LED4 oreint down
MSB	PHYAD4 = 1	Default		Depopulate [R49]
MSB	PHYAD4 = 0			Populate [R49]

PHY address '11111' = 0x1F = 31d

* Note: The (i) designates industrial temperature LAN8700i PHY (-40c to +85c). For industrial temperature applications, SMSC recommends using the LAN8700i with industrial temperature magnetics. For Commercial temperature magnetics, capacitor C1 and C4 can be depopulated. Plese refer to APP note 8.13 Magnetics Selection Guide".

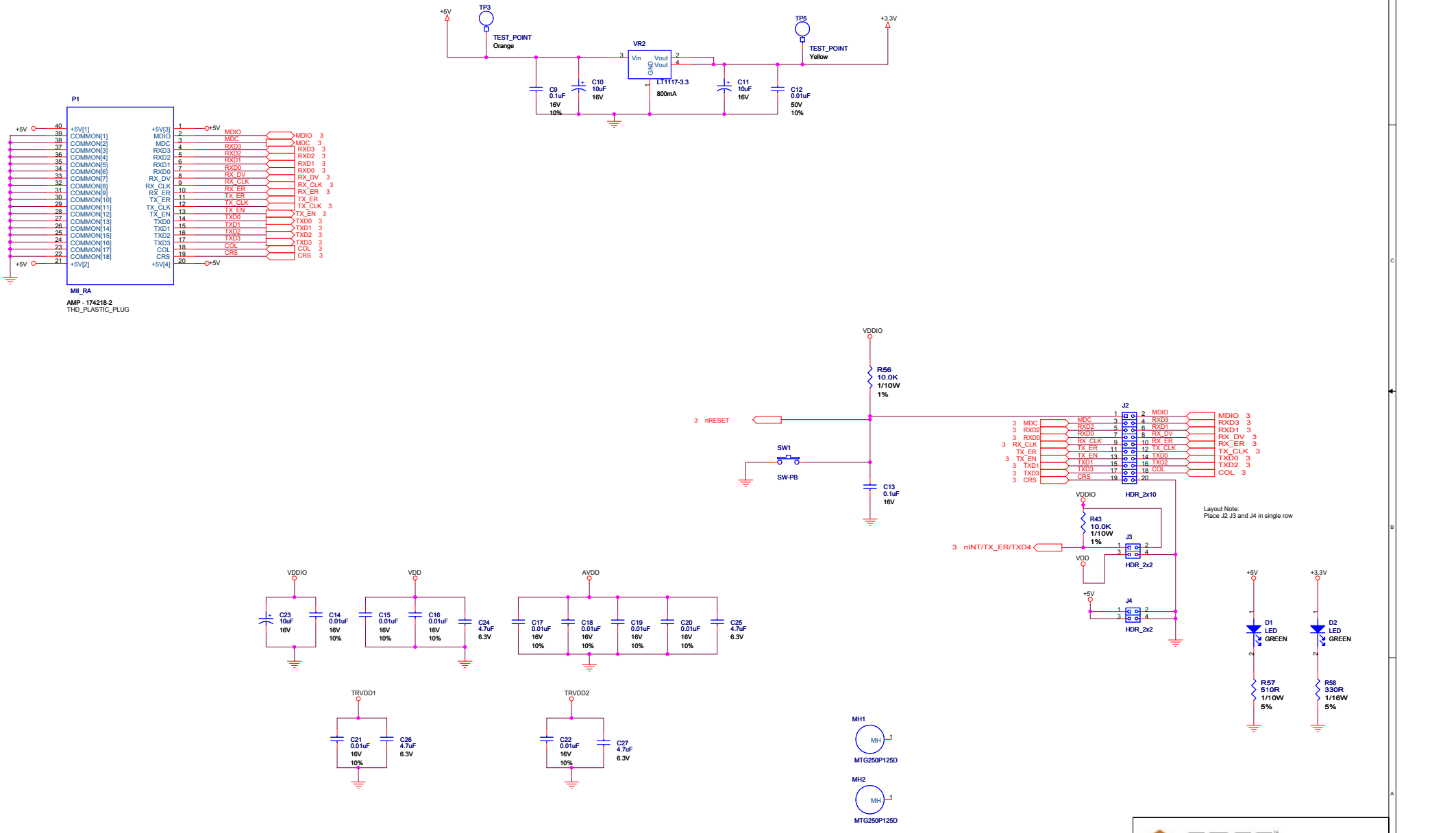
configuration resistor compliments

SMSC SUCCESS BY DESIGN
3930 East Ray Road
Suite 200
Phoenix, Arizona 85044
480-759-0200

Title	LAN8700(I) MII EVB	
Size C	Document Number SCH-7054AZ	Rev E0P1
Date: Wednesday, January 06, 2010	Sheet 3 of 4	

+5V MII to +3.3V Regulator

1.5 A Max Current from Reg



SMSC SUCCESS BY DESIGN
3930 East Ray Road
Suite 200
Phoenix, Arizona 85044
480-759-0200

Title	LAN8700(I) MII EVB	
Size C	Document Number SCH-7054AZ	Rev E0P1
Date: Wednesday, January 06, 2010	Sheet 4 of 4	