LAN9420 128VTQFP PCI Customer Evaluation Board

Assy 6492

PCB Revision A

Schematic Revision 1.2

Design Details

Board:
Assy 6492

Chip:
SMSC LAN9420

Board Form Factor:
PCI

Assembly:
128-Pin VTQFP

Circuit Diagrams utilizing SMSC Products Are Included As A Means Of Illustrating Typical Semiconductor Applications: Consequently Complete Information Sufficient For Construction Purposes Is Not Necessarily Given. The Information Has Been Carefully Checked And Is Believed To Be Entirely Reliable. However, No Responsibility Is Assumed For Inaccuracies. Furthermore, Such Information Does Not Convey To The Purchaser Of The Semiconductor Devices Described Any License Under The Patent Rights Of SMSC Or Others. SMSC Reserves The Right To Make Changes At Any Time In Order To Improve Design And Supply The Best Product Possible.

Revision History

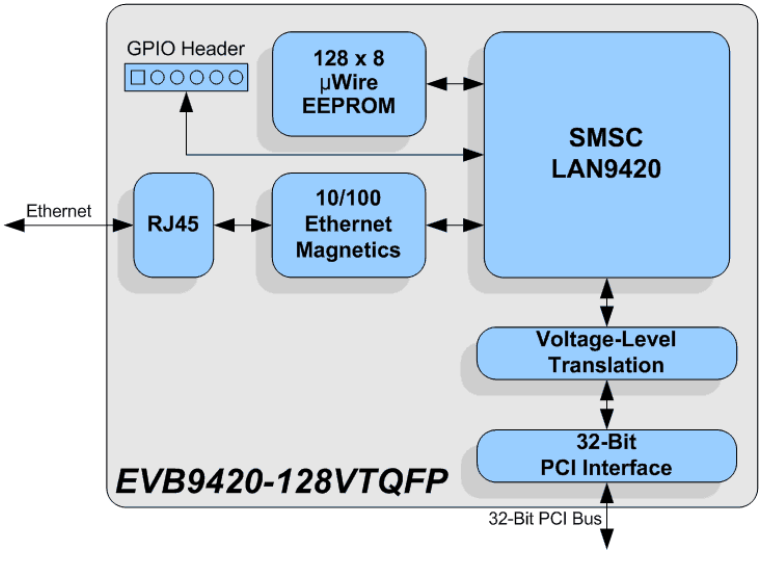
Rev 1.0 to 1.1:

Page 2: Added note for optional EMI caps C81-C84.

Rev 1.1 to 1.2:

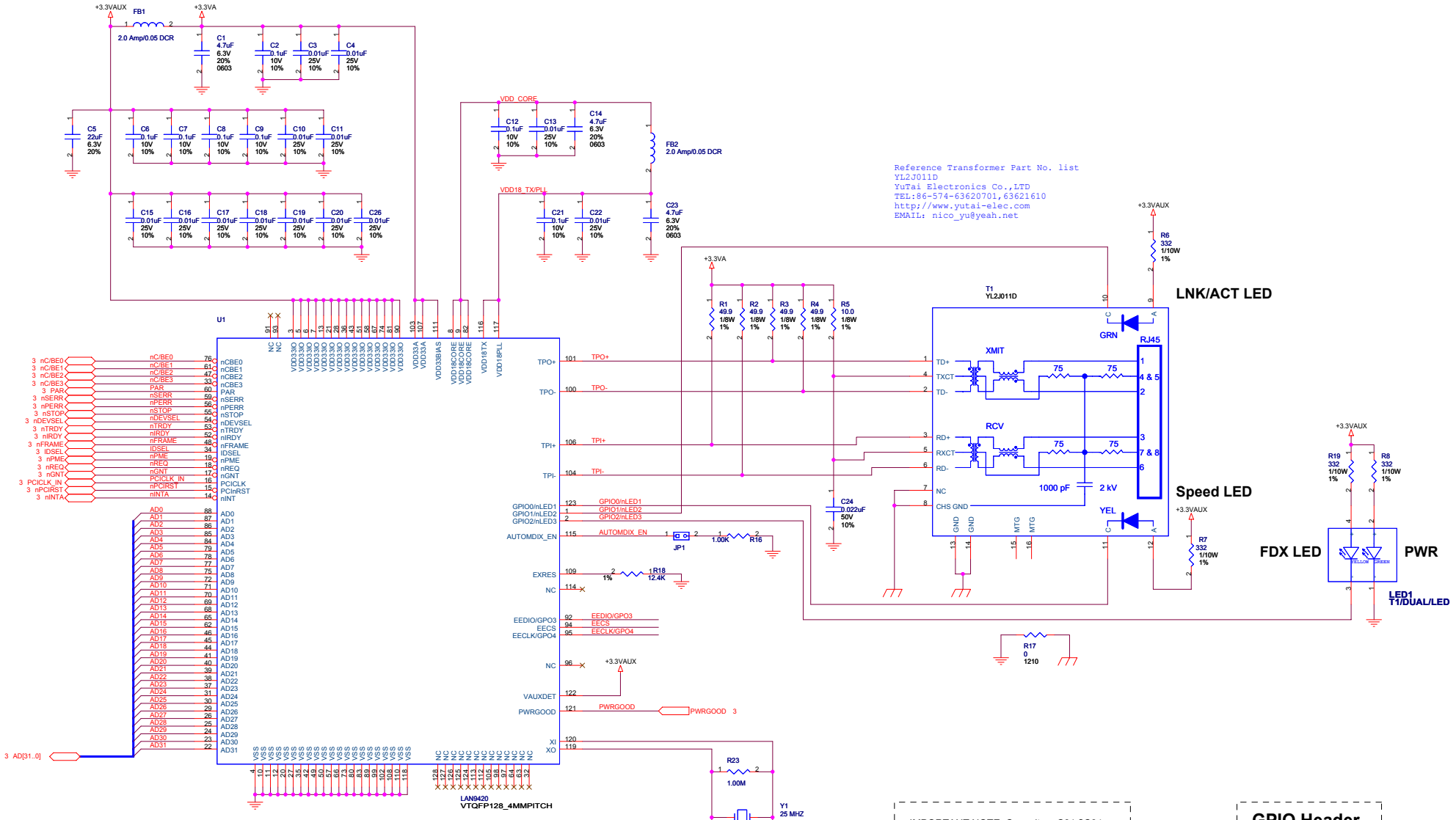
Page 2: Added note for EEPROM CS pull-down resistor.

BLOCK DIAGRAM

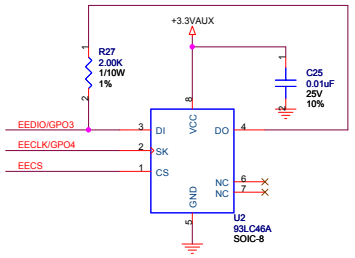


ITEM	Page(s)
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LAN9420, Ethernet, EEPROM, GPIO	2
PCI Edge Fingers and Q-Switches	3

Title: LAN9420 128VTQFP PCI Customer Evaluation Board				
Size: C	Engineer: J.M.	Assembly No.: 6492	PCB Rev: A	Schematic Rev: 1.2
Date: Wednesday, January 06, 2010			Sheet 1 of 3	

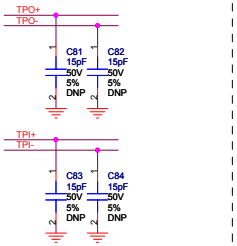


Microwire Serial EEPROM (Optional)

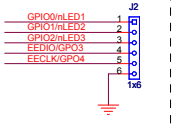


NOTE:
A pull-down resistor on the EEPROM's chip select (CS) signal is recommended by many EEPROM manufacturers. Please refer to the EEPROM manufacturer's data sheet for further information.

IMPORTANT NOTE: Capacitors C81 ?C84 are optional and are not present on the Customer Evaluation Board. These capacitors are required for operation in an EMI constrained environment. When used, these capacitors must be placed close to the transformer.

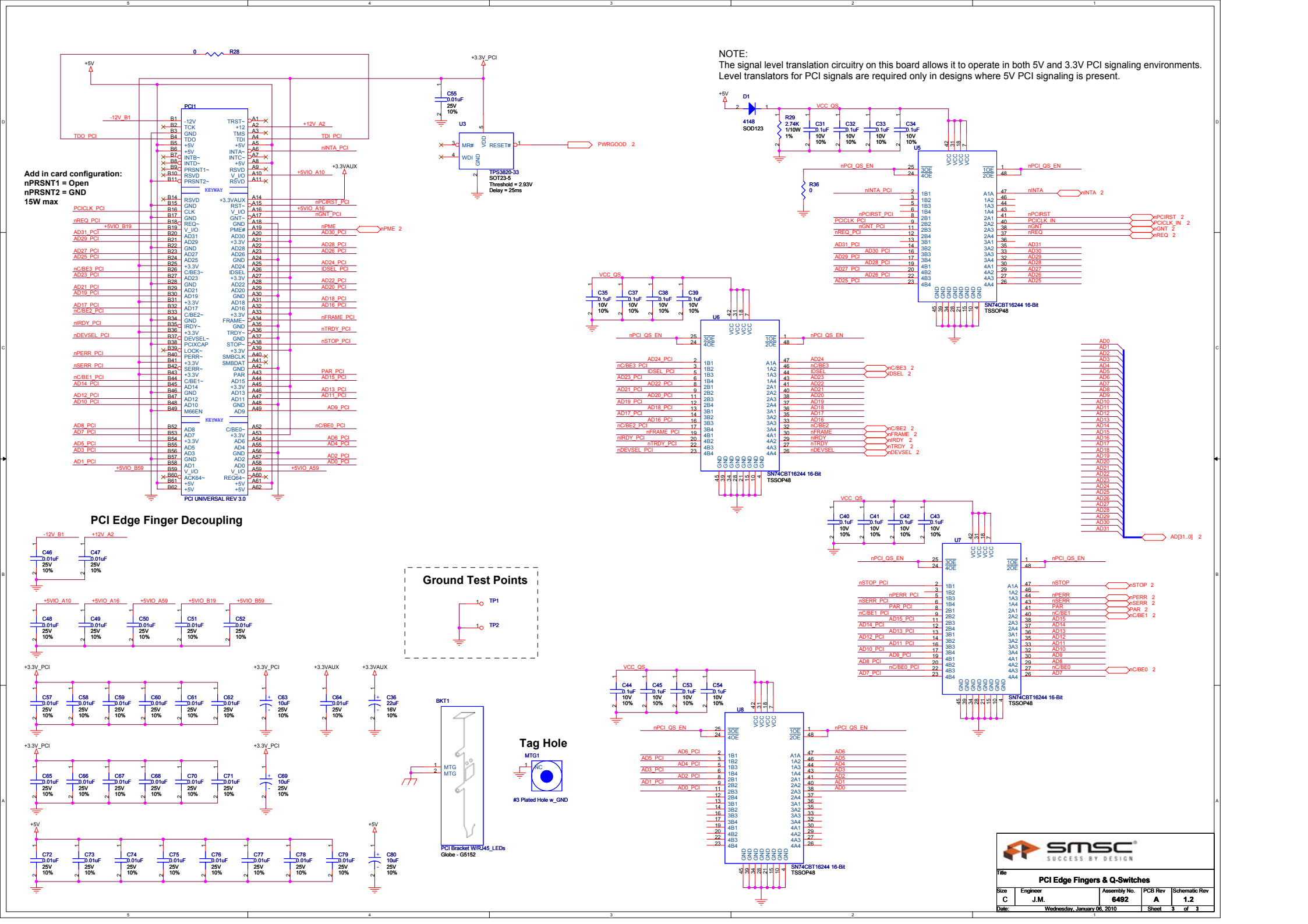


GPIO Header



SMSC SUCCESS BY DESIGN

Title				
LAN9420, Ethernet, EEPROM				
Size	Engineer	Assembly No.	PCB Rev	Schematic Rev
C	J.M.	6492	A	1.2
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NOTE:
The signal level translation circuitry on this board allows it to operate in both 5V and 3.3V PCI signaling environments.
Level translators for PCI signals are required only in designs where 5V PCI signaling is present.
Add in card configuration:
nPRSNT1 = Open
nPRSNT2 = GND
15W max
PCI Edge Finger Decoupling
Ground Test Points
Tag Hole
#3 Plated Hole w_GND
PCI Bracket W/RJ45_LEDs
Globe - G5152
PCI UNIVERSAL REV 3.0
SN74CBT16244 16-Bit
TSSOP48
TPS3820-33
SOT23-5
Threshold = 2.93V
Delay = 25ms
SMSC
SUCCESS BY DESIGN
Title
PCI Edge Fingers & Q-Switches
Size C
Engineer J.M.
Assembly No. 6492
PCB Rev A
Schematic Rev 1.2
Date: Wednesday, January 06, 2010
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